LISTING OF CLAIMS

1. (Original) A programmable flip-flop for outputting data, the flip-flop including:

a first latch for latching a first input value in response to a rising edge of a clock signal;

a second latch for latching a second input value in response to a falling edge of the clock signal;

selection means controlled by the clock signal for selectively supplying outputs of the first and second latches to the input of a third latch;

third latch control means accepting as inputs the clock signal and an inverted clock signal;

the programmable flip-flop being configurable to operate in at least first and second modes selectable by the selection means and third latch control means, such that in the first mode the output of the third latch is the first and second input values multiplexed together and output at twice the clock rate, and in the second mode one of the first and second latches is disconnected from the third latch such that the programmable flip-flop operates as a single edge-triggered register clocking out one of the first and second input values from the third latch.

2. (Original) The programmable flip-flop according to claim 1, wherein the selection means includes a first switch connecting the output of the second latch to the input of the third latch, the first switch being controlled by the clock signal such that when the clock signal is high, the first switch is closed, thereby connecting the second latch to the third latch, and when the clock signal is low, the first switch is open, thereby disconnecting the third latch from the second latch.

3. (Original) The programmable flip-flop according to claim 1, wherein the selection means includes a second switch connecting the output of the first latch to the input of the third latch, the switch being controlled by logic circuitry that accepts the clock signal and at least one programmable memory element as inputs, such that:

in the first mode, the programmable memory element is asserted, causing the clock signal to control the second switch such that when the clock signal is low, the switch is closed, thereby connecting the first latch to the third latch, and when the clock signal is high, the switch is open, thereby disconnecting the third latch from the second latch; and

in the second mode, the programmable memory element is not asserted, causing the second switch to isolate the first latch from the third latch.

4. (Original) The programmable flip-flop according to claim 1, wherein the third latch control means is a selection block for selectively supplying the inverted or non-inverted clock signal to a clock input of the third latch.

5. (Original) An input/output block, having a programmable flip-flop comprising:

a first latch for latching a first input value in response to a rising edge of a clock signal;

a second latch for latching a second input value in response to a falling edge of the clock signal;

selection means controlled by the clock signal for selectively supplying outputs of the first and second latches to the input of a third latch;

third latch control means accepting as inputs the clock signal and an inverted clock signal;

the programmable flip-flop being configurable to operate in at least first and second modes selectable by the selection means and third latch control means, such that in the first mode the output of the third latch is the first and second input values multiplexed together and output at twice the clock rate, and in the second mode one of the first and second latches is disconnected from the third latch such that the programmable flip-flop operates as a single edge-triggered register clocking out one of the first and second input values from the third latch; and

further including first input selection means and second input selection means, the first and second input selection means being selectable such that a first data value supplied to the first input selection means can be output as the first input value or the second input value, and a second data value supplied to the second input selection means can be output as the first input value of the second input value.

6. (Original) The input/output block according to claim 5, wherein operation of the first and second input selection blocks is controlled by the values of one or more configuration memory elements.

7. (Original) The input/output block according to claim 5, further including an output buffer for buffering the output of the third latch and supplying it to an interface pad.

8. (Original) The input/output block according to claim 7, wherein the buffer is a tristate buffer.

9. (Original) The input/output block according to claim 7, further including an input section, the programmable interface block including at least a third mode, in which data is accepted as input via the interface pad.

10. (Original) The input/output block according to claim 5, wherein the input values are from a functional block on the same chip as the interface block.

11. (Original) The input/output block according to claim 10, wherein the functional block comprises field programmable logic.

12. (Original) A field programmable gate array circuit incorporating an input/output block comprising:

a programmable flip-flop which comprises:

a first latch for latching a first input value in response to a rising edge of a clock signal;

a second latch for latching a second input value in response to a falling edge of the clock signal;

selection means controlled by the clock signal for selectively supplying outputs of the first and second latches to the input of a third latch;

third latch control means accepting as inputs the clock signal and an inverted clock signal;

the programmable flip-flop being configurable to operate in at least first and second modes selectable by the selection means and third latch control means, such that in the first mode the output of the third latch is the first and second input values multiplexed together and output at twice the clock rate, and in the second mode one of the first and second latches is disconnected from the third latch such that the programmable flip-flop operates as a single edge-triggered register clocking out one of the first and second input values from the third latch.

13. (Original) The gate array circuit of claim 12 further including first input selection means and second input selection means, the first and second input selection means being selectable such that a first data value supplied to the first input selection means can be output as the first input value or the second input value, and a second data value supplied to the second input selection means can be output as the first input value of the second input value.

14. (New) A data output circuit, comprising:

a first input for receiving a first input value;

a second input for receiving a second input value;

a control input for receiving a mode selection value;

a data output;

a clocked data latching circuit connected to the first, second, third and control inputs and the data output, the data latching circuit operable responsive to a first mode selection value in a

first mode to generate at the data output the first and second input values multiplexed together at twice a clock rate, and further operable responsive to a second mode selection value in a second mode to generate at the data output one of the first and second input values at the clock rate.

15. (New) The circuit of claim 14 wherein the clocked data latching circuit comprises:

a first latch for latching the first input value in response to a first edge of a clock signal;

a second latch for latching the second input value in response to a second edge of the clock signal;

a third latch having an output connected to the data output;

a selection circuit that selectively supplies outputs of the first and second latches to an input of the third latch in accordance with the mode selection value and the clock signal.

16. (New) The circuit of claim 15 further comprising a third latch clock control circuit that selectively supplies a clock and inverted clock to a clock input of the third latch in accordance with the mode selection value.

17. (New) The circuit of claim 15 wherein the selection circuit comprises:

a first switch selectively connecting the first latch output to the third latch input; and

a second switch selectively connecting the second latch output to the third latch input.

18. (New) The circuit of claim 17 wherein the first switch is controlled by the clock signal such that when the clock signal is first state, the first switch is closed to connect the second latch to the third latch, and when the clock signal is in a second state, the first switch is open to disconnect the third latch from the second latch.

19. (New) The circuit of claim 17 wherein the second switch is controlled by a logic circuit responsive to the clock signal and the mode selection value such that:

in the first mode, the second switch is closed when the clock signal is in the second state to connect the first latch to the third latch, and the second switch is open when the clock signal is in the first state to disconnect the third latch from the second latch; and

in the second mode, the second switch disconnects the first latch from the third latch.

20. (New) The circuit of claim 14 wherein the mode selection value is a multi-bit value.

21. (New) The circuit of claim 14 wherein the data output circuit is part of an input/output circuit connected to a pad.

22. (New) The circuit of claim 14 wherein the data output circuit is implemented as an integrated circuit.

23. (New) The circuit of claim 22 wherein the integrated circuit is a field programmable gate array.

24. (New) The circuit of claim 14 further including:

a first multiplexer having a plurality of data inputs and an output;

a second multiplexer having a first input coupled to the first multiplexer output and a second input coupled to the data output, the second multiplexer further having an output; and

a buffer having an input coupled to the second multiplexer output and an output coupled to an integrated circuit pad.

25. (New) The circuit of claim 24 wherein the pad is an input/output pad.

26. (New) The circuit of claim 24 wherein the plurality of data inputs to the first multiplexer include a first data input receiving the first input value and a second data input receiving the second input value.

27. (New) The circuit of claim 24 wherein the buffer is a tristate buffer and the circuit further comprises a tristate operation control circuit connected to the tristate buffer.